



PATENT APPLICATION

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Pre 1/16/05
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Kazumasa HASEGAWA et al.

Application No.: 09/934,550

Filed: August 23, 2001

Docket No.: 110450

For: FERROELECTRIC MEMORY DEVICE, METHOD OF
MANUFACTURING THE SAME, AND EMBEDDED DEVICE

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Page 2, line 25 to page 3, line 4, delete current paragraph and insert therefor:

A.1
(1) The ferroelectric layer may be disposed linearly along the first signal electrodes. Specifically, the ferroelectric layer may be selectively disposed over the first signal electrodes. In this case, since the ferroelectric layer is formed linearly along the first signal electrodes, the parasitic capacitance or load capacitance of the second signal electrodes can be decreased.

Page 3, line 22 to page 4, line 1, delete current paragraph and insert therefor:

A.2
(2) The ferroelectric layer may be disposed linearly along the second signal electrodes. Specifically, the ferroelectric layer may be selectively disposed under the second signal electrodes. In this case, since the ferroelectric layer is formed linearly along the